AMENDMENTS TO THE CLAIMS

1. (Original) A data communications system including a bidirectional buffer coupled among a transmitter, a receiver, and a transmission line, wherein the bidirectional buffer comprises:

an input differential amplifier section including two or more differential amplifiers,

wherein a first differential amplifier generates positive polarity data signals from a difference between a positive polarity transmission line signal and a positive polarity transmitter signal,

wherein a second differential amplifier generates negative polarity data signals from a difference between a negative polarity transmission line signal and a negative polarity transmitter signal,

wherein common mode rejection is independently controlled in each of the first and second differential amplifiers using bias signals generated in response to an output common mode feedback voltage from the first and second differential amplifiers; and

an output differential amplifier section that generates an output logic signal from the positive polarity data signals and the negative polarity data signals, wherein the output logic signal represents data received on the transmission line, wherein input noise is suppressed using an asymmetric transfer characteristic that offsets output signal logic levels with regard to input noise.

2. (Original) The data communications system of claim 1, further comprising a difference section coupled to receive transmission line differential signals and transmitter differential signals, wherein the difference circuitry generates signals representative of the difference between a positive polarity transmission line signal and a positive polarity transmitter signal and signals representative of the difference between a negative polarity transmission line signal and a negative polarity transmitter signal.

3. (Original) The data communications system of claim 1, wherein each of the first and second differential amplifiers include common mode feedback circuitry controlled by the output common mode of the corresponding differential amplifier to generate a feedback voltage that suppresses the common mode gain of the corresponding differential amplifier, wherein the common mode rejection of the corresponding differential amplifier is increased.

4. (Original) The data communications system of claim 1, wherein the transfer characteristic is skewed using an asymmetrical transistor configuration at an output side of a differential pair that forms the output differential amplifier section, wherein the input noise introduced by a floating input is suppressed.

5. (Original) The data communications system of claim 1, wherein symmetry is controlled in characteristics of the output logic signal using at least one logic gate with a higher logic threshold voltage than a mid-supply voltage of the output differential amplifier section, wherein a diode-connected metal-oxide semiconductor field-effect transistor (MOSFET) is placed in a ground path of the at least one logic gate.

6. (Original) A bidirectional bridge circuit for interfacing between a transmission line and a communication device, the bidirectional bridge circuit comprising:

a front-end circuit including a differential coupling to the transmission line and a differential coupling to the communication device, wherein the front-end circuit subtracts differential signals of the communication device from differential signals of the transmission line to generate a positive polarity difference signal and a negative polarity difference signal;

an amplifier circuit including a first differential amplifier and a second differential amplifier, wherein the first differential amplifier is coupled to amplify the positive polarity difference signal and generate a positive polarity data signal, wherein the second differential amplifier is coupled to amplify the

negative polarity difference signal and generate a negative polarity data signal; and

an output differential amplifier coupled to receive the positive polarity data signal and the negative polarity data signal and generate an output logic signal representative of data received via the transmission line.

7. (Original) The bridge circuit of claim 6, wherein common mode rejection is independently controlled in each of the first and second differential amplifiers using bias signals generated in response to an output common mode feedback voltage from the first and second differential amplifiers.

8. (Original) The bridge circuit of claim 6, wherein the first differential amplifier includes common mode feedback circuitry controlled by the output common mode of the first differential amplifier to generate a feedback voltage that suppresses the common mode gain of the first differential amplifier, wherein the common mode rejection of the first differential amplifier is increased.

9. (Original) The bridge circuit of claim 6, wherein the second differential amplifier includes common mode feedback circuitry controlled by the output common mode of the second differential amplifier to generate a feedback voltage that suppresses the common mode gain of the second differential amplifier, wherein the common mode rejection of the first differential amplifier is increased.

10. (Original) The bridge circuit of claim 6, wherein the output differential amplifier suppresses input noise using an asymmetric transfer characteristic that offsets output signal logic levels with regard to input noise.

11. (Original) The bridge circuit of claim 6, wherein the output differential amplifier suppresses noise introduced by a floating input using an asymmetric transfer characteristic, wherein the output differential amplifier transfer characteristic is skewed

using an asymmetrical transistor configuration at an output side of a differential pair that forms the output differential amplifier.

12. (Original) The bridge circuit of claim 6, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a threshold voltage that is higher than a mid-supply voltage of the output differential amplifier.

13. (Original) The bridge circuit of claim 6, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a higher input threshold voltage than a mid-supply voltage of the output differential amplifier, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a ground path of the at least one logic gate.

14. (Original) The bridge circuit of claim 6, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a lower input threshold voltage than a mid-supply voltage of the output differential amplifier, wherein a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) is placed in a supply path of the at least one logic gate.

15. (Original) The bridge circuit of claim 6, wherein the output differential amplifier comprises a NAND logic gate with a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path, wherein a logic threshold voltage of the NAND logic gate is higher than a mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

16. (Original) At least one semiconductor chip having a bidirectional bridge connecting each of a transmitter and a receiver to a transmission line, wherein the bidirectional bridge comprises:

a first differential amplifier that generates positive polarity data signals from a difference between a positive polarity transmission line signal and a positive polarity transmitter signal; and

a second differential amplifier that generates negative polarity data signals from a difference between a negative polarity transmission line signal and a negative polarity transmitter signal;

common mode feedback circuitry that independently controls common mode rejection in the differential amplifiers via bias signals generated in response to an output common mode feedback voltage from the first and second differential amplifiers, wherein an output logic signal is generated from the positive polarity data signals and the negative polarity data signals that represents data received on the transmission line.

17. (Original) A bidirectional communications system comprising:

at least one transmitter;

at least one receiver; and

at least one buffer coupling the at least one transmitter and the at least one receiver to at least one transmission line, the at least one buffer comprising:

difference circuitry coupled to receive transmission line differential signals and transmitter differential signals, wherein the difference circuitry generates positive polarity and negative polarity difference signals by subtracting the transmitter differential signals from the transmission line differential signals;

amplifier circuitry including a first differential amplifier and a second differential amplifier,

wherein the first differential amplifier receives the positive polarity difference signals and generates positive polarity data signals, and

wherein the second differential amplifier receives the negative polarity difference signals and generates negative polarity data signals; and

output circuitry that amplifies and combines corresponding positive and negative polarity data signals to generate single-ended logic signals representative of data received on the transmission line, wherein the logic signals are coupled to the receiver.

18. (Cancelled)

19. (Original) A method for providing a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line, the method comprising:

generating positive and negative polarity data signals using separate differential amplifiers that receive differential signal pairs from each side of a differential link to the transmission line and the transmitter;

independently controlling common mode rejection in each of the separate differential amplifiers using bias signals generated in response to an output common mode feedback voltage from each of the differential amplifiers;

generating output logic signals representing data received on the transmission line using the positive polarity data signals and the negative polarity data signals;

suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic;

controlling symmetry in switching transients of the output logic signals by increasing a logic threshold voltage of a logic gate of the output amplifier above a mid-supply voltage of the logic gate; and

providing the output logic signals to the receiver.

20. (Original) The method of claim 19, wherein controlling common mode rejection comprises:

receiving a common mode output voltage from a differential amplifier; generating a common mode feedback voltage using the common mode output voltage; and

suppressing a common mode gain of the differential amplifier in response to the common mode feedback voltage, wherein the common mode rejection of the differential amplifier is increased.

21. (Cancelled)

22. (Original) A method for providing a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line, the method comprising:

receiving differential pairs of signals from the transmission line and the transmitter;

generating an output logic signal to the receiver;

suppressing effects of input noise from a floating input on the output logic signal by skewing a transfer characteristic of an output amplifier; and

controlling symmetry in switching transients of the output logic signal by increasing a logic threshold voltage of a logic gate of the output amplifier above a mid-supply voltage of the logic gate.

23. (Original) A computer readable medium including executable instructions which, when executed in a processing system, provide a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line by:

generating positive and negative polarity data signals using separate differential amplifiers that receive differential signal pairs from each side of a differential link to the transmission line and the transmitter;

independently controlling common mode rejection in each of the separate differential amplifiers using bias signals generated in response to an output common mode feedback voltage from each of the differential amplifiers;

generating output logic signals representing data received on the transmission line using the positive polarity data signals and the negative polarity data signals;

suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic;

controlling symmetry in switching transients of the output logic signals by increasing a logic threshold voltage of a logic gate of the output amplifier above a mid-supply voltage of the logic gate; and

providing the output logic signals to the receiver.

24. (Original) A bidirectional communication link, comprising:

means for receiving transmission line differential signal pairs;

means for receiving transmitter differential signal pairs;

means for generating positive polarity data signals from a difference between a positive polarity transmission line signal and a positive polarity transmitter signal;

means for generating negative polarity data signals from a difference between a negative polarity transmission line signal and a negative polarity transmitter signal;

means for controlling common mode rejection during data signal generation by generating bias signals in response to an output common mode feedback voltage;

means for generating an output logic signal from the positive polarity data signals and the negative polarity data signals, wherein the output logic signal represents data received in the transmission line differential signal pairs; and

means for coupling the output logic signal to a receiver.